

***Light On Board*[™] Optically Enabled BGA IC Package**

Prototype Results

This white-paper consists of two major sections; the first is the physical description of this prototype Optically Enabled BGA (OEBGA) IC Package, and the second is a preliminary performance characterization of the IC package – both electrically and optically.

The design of the OEBGA IC Package was done exclusively by Reflex Photonics Inc. – this includes all the sub-component design used in the package (except for the driver/receiver ASIC chips and the VCSEL laser/PD chips – these were purchased from vendors) where external suppliers were used to manufacture semi-custom sub-components. The *LightABLE*[™] optical sub-assemblies (OSAs) embedded in the OEBGA IC Package are proprietary to Reflex Photonics Inc. and were assembled in-house. The general design for the metal housing, the interposer substrate as well as the strategy for wirebonding, chip placement and glob-topping are all based on the criterion outlined in most JEDEC packaging specifications. The final assembly steps for this package were carried out by an industry-leading semiconductor packaging and test facility on volume production machinery – to prove out the manufacturability of this type of package.

1. Description of the Prototype OEBGA IC Package

The OEBGA IC Package is a cavity-down, ball grid-array (BGA), that is 45-mm x 45-mm x 4.5-mm in size with 600 solder balls and 2 optical ports, providing 12 optical channels with each of the 2 ports. It is composed of a metal housing laminated to a patterned substrate (or interposer) circuit board that has a total of 600 solder balls arranged in a 35x35 regular array pitched at 1.27-mm (5 columns and 5 rows deep), a glob-topping epoxy, wirebonds, and two (2) twelve (12) channel *LightABLE*[™] optical sub-assemblies (OSA's) that contain: optical fibers, lasers/photodetectors, alignment ferrules and external optical interfaces, this is shown in [figure 01](#). The OEBGA also contains two microchips used for this evaluation – a 12 channel laser-driver chip and a 12 channel photodetector-receiver chip; these are used to exercise the laser and photodetector chips, respectively.

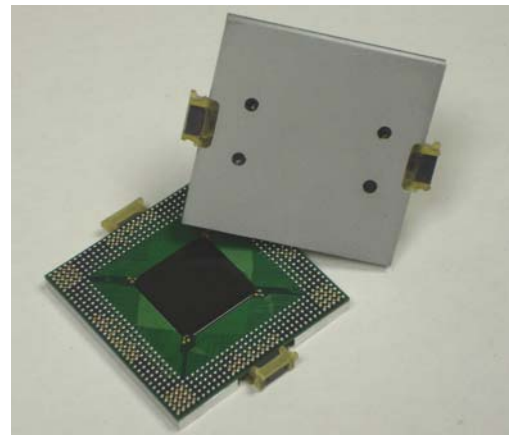


Figure 01: OEBGA Prototype IC Package

IC Package Chip Cavity:

The cavity-down orientation refers to the side on which the microchips are placed – the cavity-down design allows the microchip to be placed on the same side as the solder ball array. This

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orientation offers the best configuration for heatsinking and power dissipation since the microchip can be mounted directly on a metal housing where the other side of the housing is exposed to air (or connected to a heatsink).

The inner cavity is 15-mm x 15-mm in area and recessed into the package by 3.5-mm. The actual area able to receive a custom microchip is 10-mm x 10-mm, where the extra 2.5-mm on each side of this area is reserved for the wirebondable areas of the optical sub-assemblies. Two levels of wirebonding are done within the cavity; the first is within the cavity between the microchip and the optical sub-assemblies, and the second is between the microchip and the fingers of the laminated patterned substrate, as shown in [figure 02](#). The wirebonds connected to the OSAs drive or receive signals from the lasers and photodetectors (producing or accepting pulses of light), and the wirebonds connected to the substrate fingers drive or receive electrical signals.

In this particular prototype experiment, the 10-mm x 10-mm cavity area for the microchips is greatly under-used. Two, much smaller, evaluation microchips are used requiring very long external wirebonds. The longest wirebonds are 8.5-mm long and are a source of noise and signal degradation. This is easily remedied by designing the package around a more appropriately sized *custom* microchip where much shorter wirebonds can be achieved.

Optical Sub-Assembly:

The two optical ports that protrude from the sides of this package are capable of 12 channels of optical input and 12 channels of optical output where each channel, in this first reference prototype, can be operated up to approximately 3.5-Gbps for an aggregate data rate of 84-Gbps. *Note that this is in addition to the electrical bandwidth provided by the IC package.*

The Reflex *LightABLE*TM Optical Sub-Assembly as shown in [figure 03](#) converts electrical signals to optical signals using a 1x12 array of GaAs 850-nm VCSELs rated for 3.5-Gbps direct modulation. The same form-factor OSA can also convert optical signals to electrical signals using a 1x12 array of GaAs 850-nm PIN photodetectors capable of at least 3.5-Gbps data rates. The OSA is optically pre-aligned and has two standard interfaces, one to connect to the

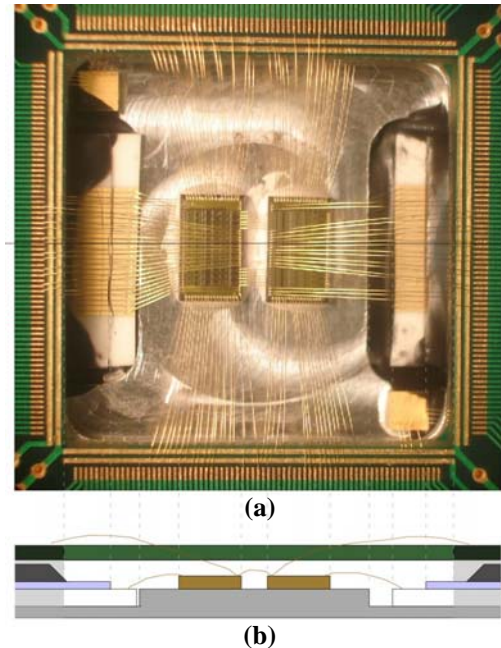


Figure 02: View of Cavity with wirebonds: a) top view b) cross-section

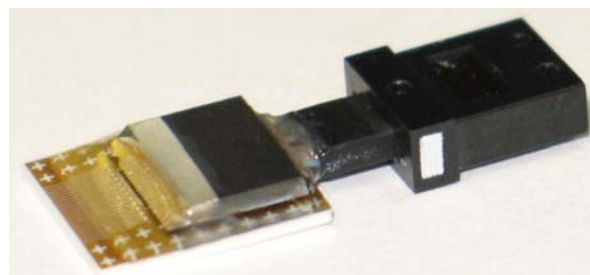


Figure 03: Reflex *LightABLE*TM Optical Sub-Assembly

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electrical signals (such as wire bond pads) and the other to connect to the optical signals (such as an optical MT connector). The OSA is placed such that the electrical connections (the bond pads) are next to the driver or receiver IC chips on the interposer board and the optical interface is protruding from the edge of the interposer board. The optical sub-assemblies are composed of an Alumina Substrate, VCSEL or PD chip, transparent epoxy, a silicon v-groove chip, optical fiber, and an MT optical ferrule, as shown in [figure 04](#).

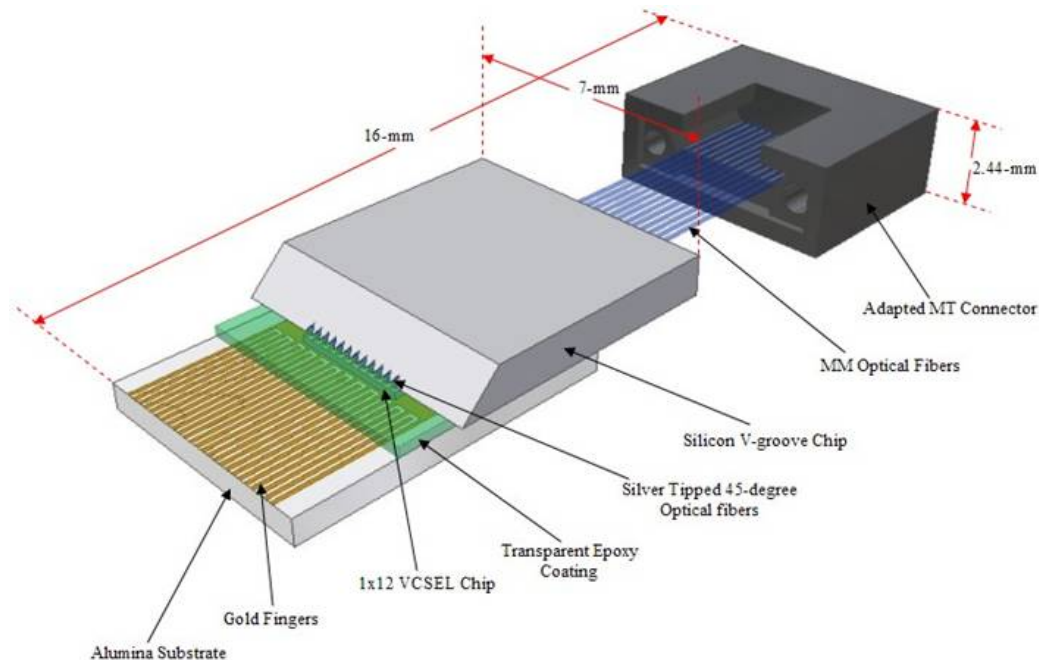


Figure 04: Mechanical drawing and sub-components of the Reflex OSA.

Optical Connector Port:

The optical interface of the OSA is the standard MT (multi-termination) optical ferrule used widely in the industry for multi-channel parallel optical fiber ribbon. The MT's optical facet, as shown in [figure 05](#), has micro-molded holes each with optical fibers and two larger alignment dowel pin holes to align MT's together. The MT optical ports that protrude from the sides are fixed in place, and an optical fiber ribbon cable terminated with an MT ferrule can be aligned to the optical ports using the dowel pins, as shown in [figure 06](#) and [07](#). A small, disposable metal spring-clip, as shown in [figure 08](#), is used to hold the MT cable to the OEBGA's optical port and applies a mating pressure from the back as it is clipped into receiving notches inside the OEBGA IC Package, as shown in [figure 09](#).



Figure 05: Front Facet of MT Ferrule

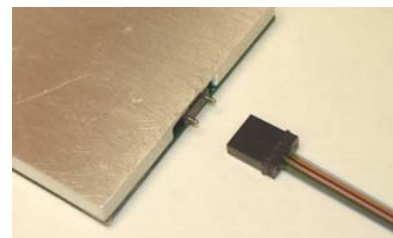


Figure 06: MT Ferrule alignment to OEBGA

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There are many aspects to this optical port and spring-clip design which contribute to the ease of assembly and reliability as well as reduced area and reduced cost.

- The standard MT optical port at the sides of the IC package allow both printed circuit board assembly steps (such as pick-and-place and solder re-flow) and do not interfere with the vertical heatsinking of typical packages. Essentially, this concept takes advantage of the unused area of the IC package – that being “the sides”.
- The optical port can be covered using a small form-fitting rubber/plastic boot (or cover) to allow standard board assembly techniques (typically handling and solder-flux fume contamination) to be used without damaging the optical facet of the MT port.
- The IC package and the optical ports are designed to have no moving features (such as springs or bendable plastic clips) so that the IC package can never “break” and render the IC package’s port “useless” – especially after the IC package has been soldered to a PCB. The MT port uses open side cavities with notches to allow for an external spring clip to hook over these notches. If the spring clip breaks or bends, the clip is simply replaced for another. Furthermore, including the alignment dowel pins on the IC package’s MT port offers a degree of protection when the optical patch cable is being connected. Also, since the MT port protrudes the side of the IC package, it offers much easier access to the optical facet for cleaning just before the final assembly of the optical cables on to the IC package.

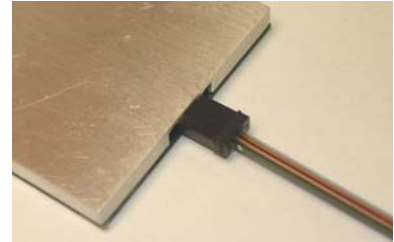


Figure 07: Aligned MT Ferrule on OEBGA

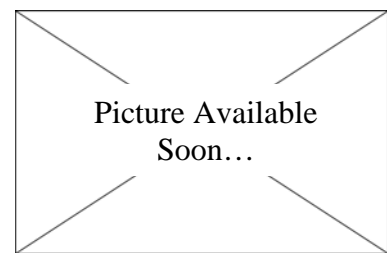


Figure 08: OEBGA MT Clip

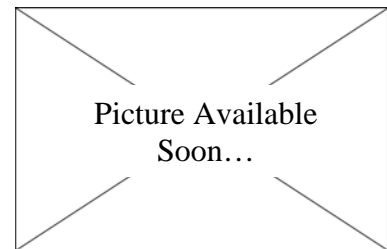


Figure 09: OEBGA Connected Optical Port

2. Electrical and Optical Characterization

In this section, the electrical performance of the prototype OEBGA IC Package is presented. It describes the data rates, rise/fall times, optical powers, sensitivity and propagation delay of the OEBGA to provide a general assessment of the performance of the OEBGA IC Package as a whole. Three fundamental tests of the OEBGA IC Package have been performed to collect this data, they are: 1) electrical-to-optical; from an electrical signal generator, through the package, to a high-speed photodetector, 2) optical-to-electrical; from an optical source of digital data, through the package, and out the electrical ports, and 3) optical-to-optical; done using three different methods to show all the possible modes of operation for the OEBGA IC Package.

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Electrical / Optical Testboard:

The OEBGA was tested using a custom testboard where the IC package was solder re-flowed to the center of the board and high-speed electrical signals were routed to and from the IC package terminated with SMA connectors on the edges of the testboard. The optical signals were accessed by connecting optical fiber ribbon cables terminated with MT ferrules to the sides of the IC package. In figure 10, the electrical connections are shown using red arrows and the optical connections are shown using blue arrows.

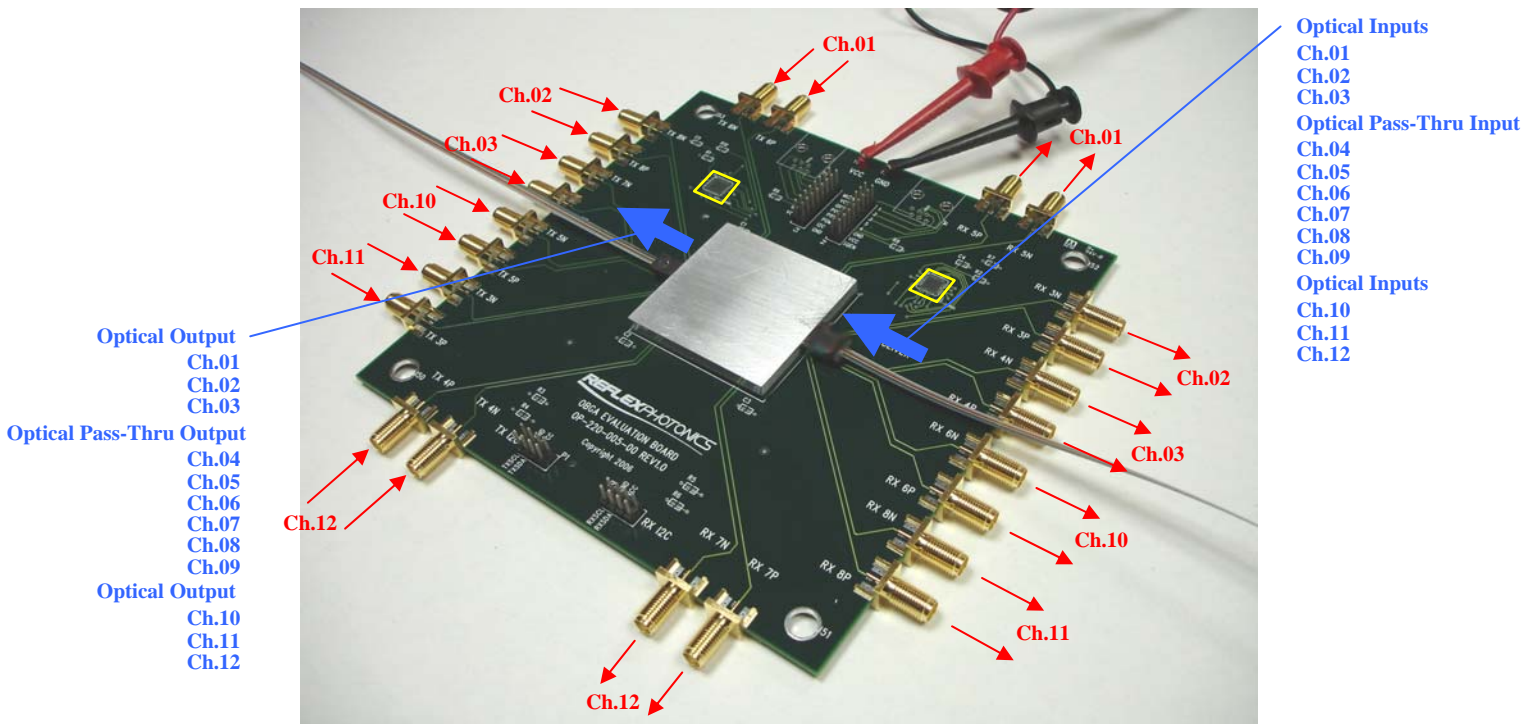


Figure 10: OEBGA Testboard – 2-optical port IC package with MT connectors and 6 input electrical / 6 output electrical SMA connectors

Note that a strategy to reduce the number of test channels was used on the testboard – since there are 12 optical input channels and 12 optical output channels; requiring a theoretical 48 SMA connectors (for differential signaling of each channel), the *optical-input to electrical-output* connections were done on channels 1,2,3,10,11 and 12. Similarly, the *electrical-input to optical-output* connections were done on channels 1,2,3,10,11, and 12. This reduced the number of SMA connectors required from 48 down to 24 – 12 for the *O-to-E* and 12 for the *E-to-O*. The middle set of channels, 4,5,6,7,8, and 9 were wirebonded between the receiver side of the package and the driver side effectively forming a “pass-thru” or an *optical-to-electrical-to-optical* connection. This set of channels required no external electrical connections and limits the physical distances during which the signals are in electrical form inside the IC package.

The driver and receiver ASIC chips that are used to directly interact with the VCSEL lasers and photodetectors within the OEBGA IC Package are programmed using microcontroller chips that

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are surface mounted on the testboard (the small yellow squares in [figure 10](#)). The microcontroller loads the registers of the driver and receiver ASIC chips to set output optical power levels and filtering. An assembler/C++ program is written into the EEPROM of the microcontrollers using an external USB/I2C bus and upon power up, the microcontroller loads the settings into the driver/receiver ASIC chips as well as supports a GUI controlled interface for digital diagnostics (through the I2C bus between a laptop running NI LabView™ and the testboard) – this also allows for real-time interrogation of the driver/receiver chips

The equipment used in the tests were an Anritsu MP1763C Data Generator and MP1764C Error Detector, the Agilent DCA-J 86100C sampling scope, the New Focus 1554-A High-speed photodetector.

The testboard was further characterized by using a “dummy” IC package that contained no microchips or OSAs and was simply wirebonded between pairs of channels. This was to assess the cross-talk, attenuation and jitter after sending differential patterns of data into and back out of the testboard as shown in [figure 11](#). As is evident by the data presented below, the testboard itself also contributes to the degradation of the data signal – this is primarily due to the materials used (FR-4) and the distance (~20-cm) traveled and actually is a very persuasive argument *for the use* of optics directly inside the IC package – to avoid these problems.

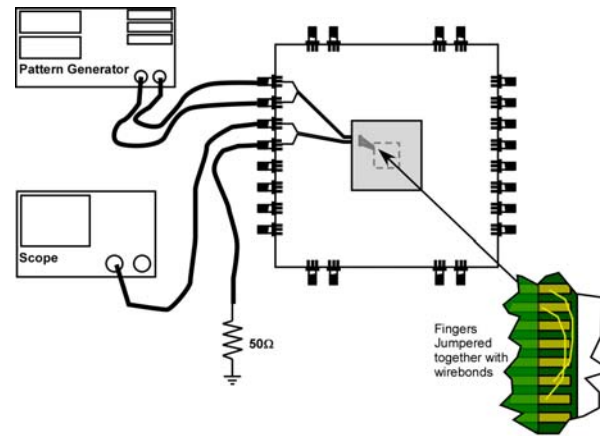


Figure 11: Test of Testboard performance using internal loop-back on “dummy” IC package

Input:

Data Pattern:	10101010 repeating pattern
Data Rate:	3.125-Gbps
Voltage Level	0V/0.4V (limited by Anritsu)
Rise/Fall Time (20/80)	30 ps / 32 ps
Total Jitter	9 ps

Output:

Voltage Level	0V/0.353V
Rise/Fall Time (20/80)	77.9 ps / 85.3 ps
Total Jitter	18 ps

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Electrical-to-Optical Characterization:

The schematic in [figure 12](#) shows the set-up for the E-to-O test, the data source was the Agilent generator and the receiver was the New Focus photodetector.

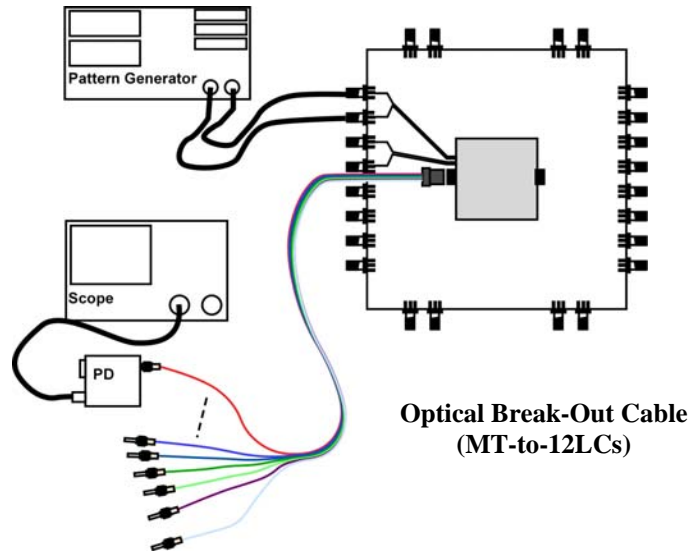


Figure 12: Test setup for E-to-O Characterization

Input:

Data Pattern:	$2^{23}-1$
Data Rate:	3.125-Gbps
Voltage Level	CML 2.0V/1.6V (limited by Anritsu)
Rise/Fall Time	30 ps / 32 ps
Total Jitter	23 ps

Output:

Optical Power (hi/lo)	0.493 mW / 0.093 mW
Extinction Ratio (measured at 550-Mhz sq. wave)	7.24 dB
Rise/Fall Time	71.1 ps / 80.0 ps
Total Jitter (approximate)	55 ps

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The figures 13 and 14 below are screen-captures of a typical eye-diagram at 3.125-Gbps (PRBS $2^{21}-1$) obtained using the New Focus photodetector and the respective rising and falling edges are derived from a square wave pattern.

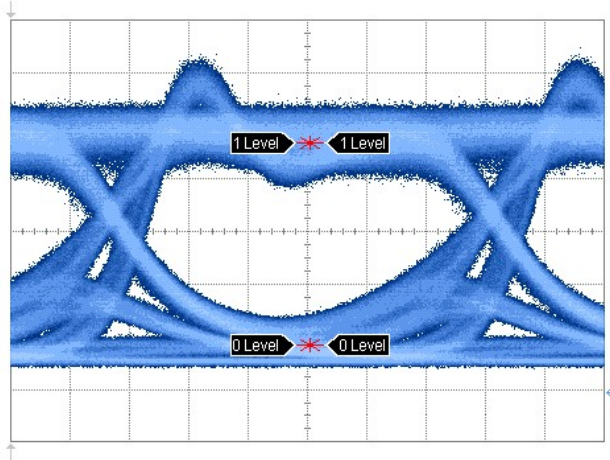


Figure 14: E-to-O Eye Diagram (3.125-Gbps PRBS $2^{23}-1$)

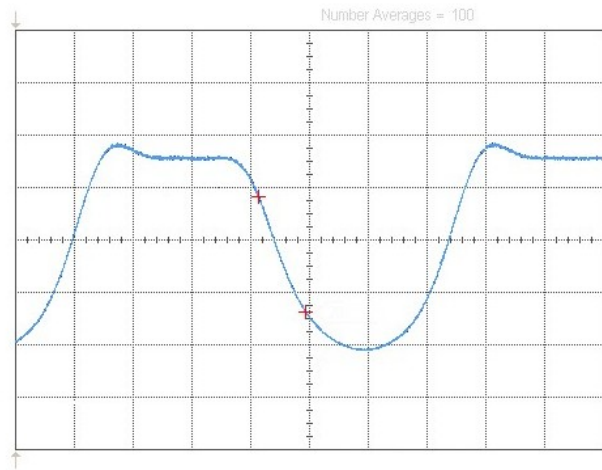


Figure 15: E-to-O Rise and Fall of a 3.125-Gbps (1010 pattern)

Optical-to-Electrical Characterization:

To produce the optical signal, the Anritsu Data Generator was used to electrically stimulate an external optical transmitter module. The optical data generated was then used as the source of optical input to the optically enabled IC package. The “input” table below is the optical data *from* the external optical transmitter module as seen by the New Focus photodetector. A typical eye-diagram is shown in figure 17 and the rise and fall curves are shown in figure 18. The schematic in figure 19 shows the set-up for the O-to-E test. This setup was somewhat more complicated due to the need for a source of optical data - shown as the “Transmitter Eval Board” (the circle with flat sides).

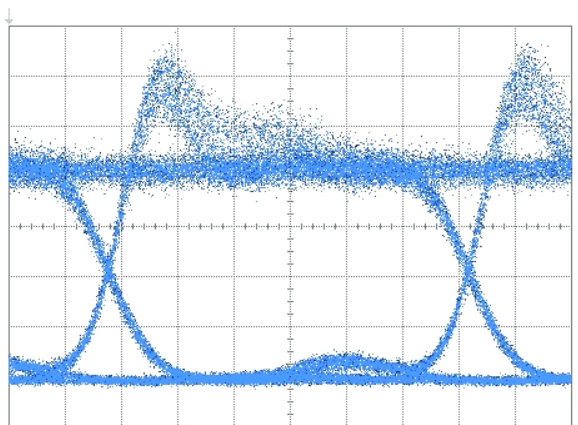


Figure 17: Optical Output Eye-Diagram (3.125-Gbps PRBS $2^{23}-1$) from an optical transmitter module – becomes the Optical Input for the OEBGA

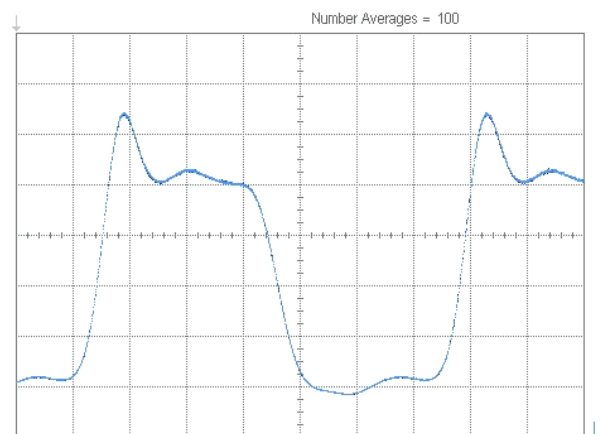


Figure 18: Optical Output Rise and Fall pattern from an optical transmitter module at 3.125-Gbps (square wave pattern)

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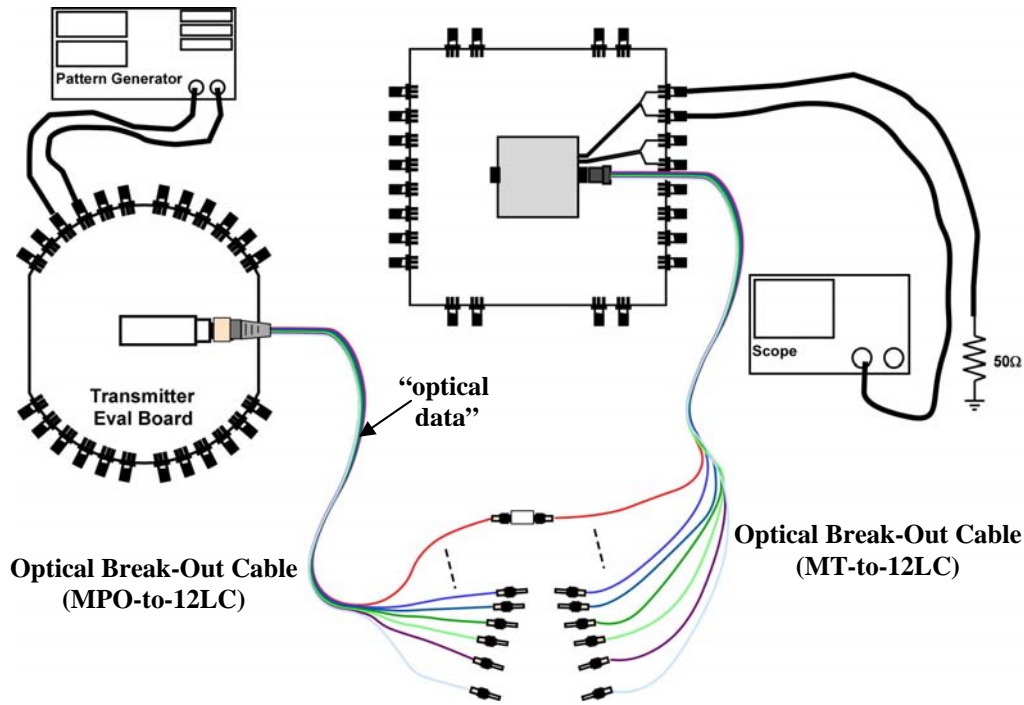


Figure 19: Test setup for O-to-E Characterization

The “output” table below is the recovered electrical signal from the OEBGA IC Package as seen directly by the Agilent sampling scope. Note that although the OEBGA IC Package’s CML driver normally output a 400-mV swing, the voltages received at the edge of the testboard’s SMA connectors have been attenuated by the FR-4 test board down to about 300-mV.

Input:

Data Pattern:	$2^{23}-1$
Data Rate:	3.125-Gbps
Optical Power (hi/lo)	0.958 mW / 0.225 mW
Extinction Ratio (measured at 550-Mhz sq. wave)	6.29 dB
Rise/Fall Time	73.5 ps / 75.5 ps
Total Jitter (approximate)	54.4 ps

Output:

Voltage Level	3.25V/3.05V (CML output)
Rise/Fall Time	90.2 ps / 80.2 ps
Total Jitter	89 ps

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The output electrical eye diagram from the OEBGA IC Package and the rising and falling edges derived from a square wave pattern at 3.125-Gbps are shown in figures 20 and 21. There is some pattern dependant jitter which is indicated by the double lines in both the rising and falling edges and can be attributed to both relaxation oscillation issues in the optical transmitter and the extremely long wirebond lengths within the IC package cavity.

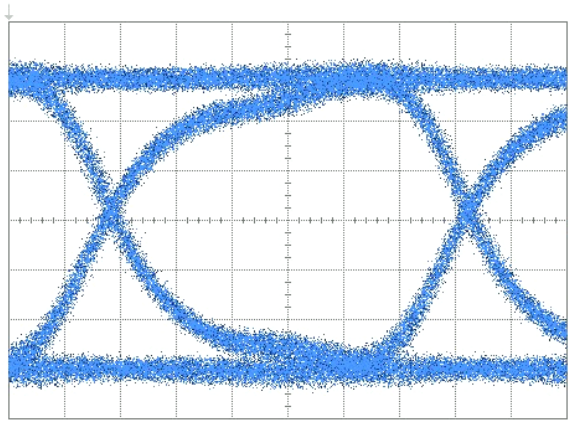


Figure 20: O-to-E Eye Diagram (3.125-Gbps PRBS 2²³-1)

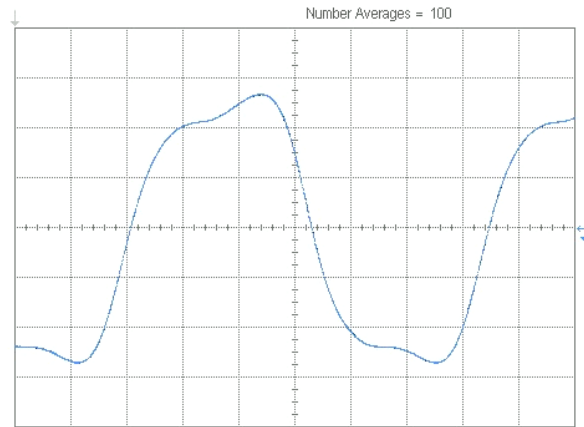


Figure 21: O-to-E Rise and Fall of a 3.125-Gbps (square wave pattern)

One further measurement of the performance of the optical-to-electrical performance within the OEBGA IC Package is the sensitivity of the optical receiver. This measurement is done by decreasing the optical power to the receiver photodetector by using an external passive optical attenuator, and then plotting the optical power incident on the photodetector versus the bit-error-rate (BER) for a given data rate and PRBS. Typically, as the optical power is decreased the BER increases as shown in figure 22. In this particular case, the SONET BER of 1e-10 is achieved at about an optical power of -15.5dBm.

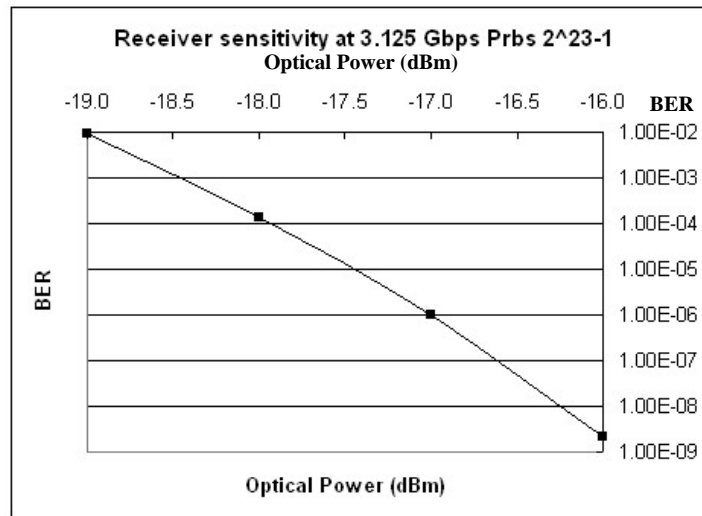


Figure 22: O-to-E Receiver Sensitivity

Optical-to-Optical Characterization:

There are three possible optical-to-optical characterizations that can be made using the OEBGA and testboard. Each of these tests are briefly presented here mainly to demonstrate the possible operational modes of an OEBGA, but also to provide valuable insight regarding the “inner-operation” of the IC package as a method for ultra-high-speed communications using the “fiber-to-the-chip” (FTTC) technology.

1) Optical-to-Optical Test – Repeater Configuration:

This optical-to-optical test setup is shown in [figure 23](#) and involves sending an external source of optical data from an external optical transmitter module (labeled “Transmitter Eval Board”), through the OEBGA IC Package and then receiving the optical data using an external optical receiver module (labeled “Receiver Eval Board”).

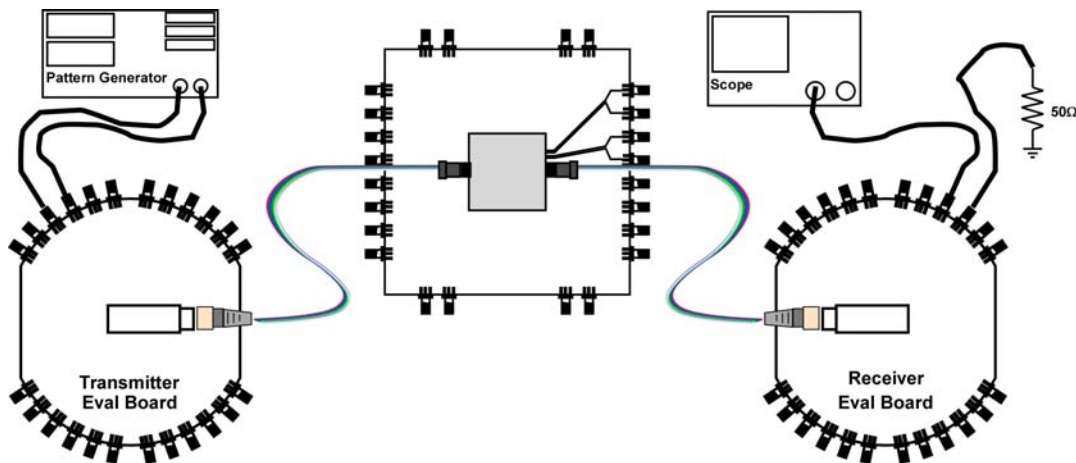


Figure 23: O-to-O Test Setup – Repeater Configuration

In this test the OEBGA receives optical data using its photodetector/receiver port and converts it to electrical data. This electrical data is then immediately sent to the driver/VCSEL port where it is converted back to optical data – this happens all within the OEBGA IC Package. This is similar to an optical repeater performing an O-to-E-to-O conversion. The final electrical eye diagram is shown in [figure 24](#) and is very similar to the O-to-E case described above, except for a slightly wider gap in the rising edges resulting in increased jitter. The increased jitter is primarily a result of the very long wirebonds described above.

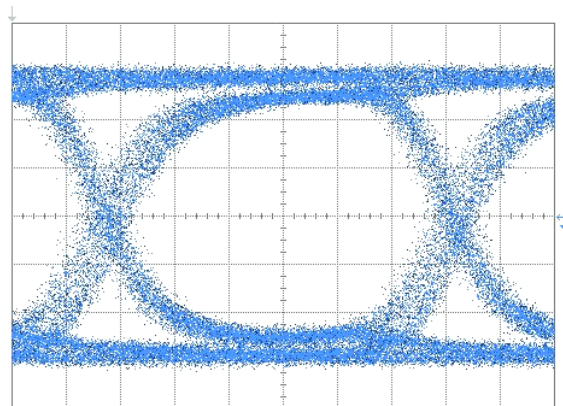


Figure 24: O-to-O Eye Diagram at 3.125-Gbps and PRBS $2^{23}-1$ for Repeater

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2) Optical-to-Optical Test – Self Loop-Back Configuration:

This optical-to-optical test setup is shown in [figure 25](#) and might equally be called an “*electrical-to-electrical*” test. Electrical data is supplied by the Anritsu Data Generator and connected to the input SMA connectors. The driver ASIC and VCSEL convert the electrical data into optical data and it is sent out the optical output port. The optical output port is fed-back into the optical input port, using a single MT-to-MT parallel optical fiber ribbon cable, whereon the optical data is converted back into electrical data using the photodetector and receiver ASIC and sent out the output SMA connectors. The pronounced double edges on the rising and falling edges of [figure 26](#) are due primarily to the non-optimal long wirebonds within the package as previously mentioned.

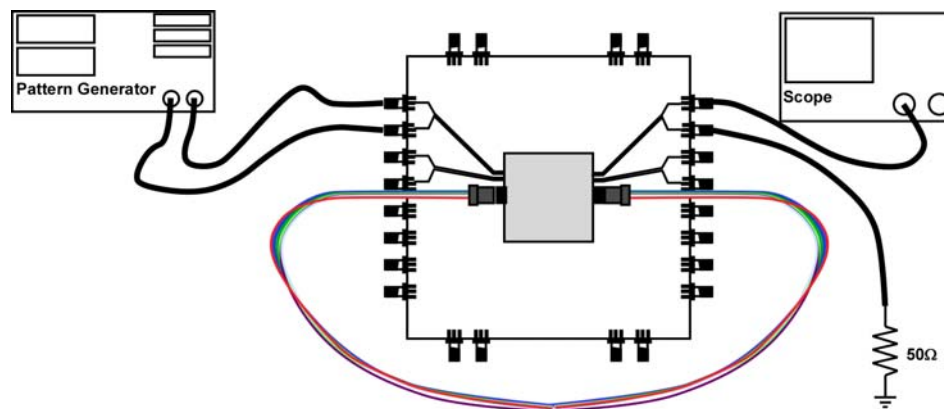


Figure 25: O-to-O Test Setup – Self Loop-Back Configuration

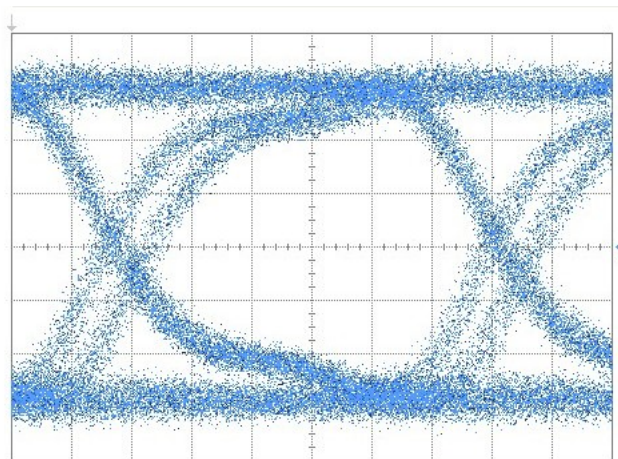


Figure 26: O-to-O Eye Diagram at 3.125-Gbps and PRBS $2^{23}-1$ for Self Loop-Back

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3) Optical-to-Optical Test – Ring Oscillator Configuration:

This test setup is perhaps one of the most interesting test feature of this OEBGA test platform. Not only does this test allow insight into the inner operation of the OEBGA IC Package (without the need for external electrical connections), but it also highlights the ability of optical signaling to achieve broadcasting while maintaining very high-speed data rates.

As described earlier on page 5, the testboard and OEBGA IC Package were designed to limit the number of required electrical test points (mostly for convenience). Some channels were reserved for simple E-to-O and O-to-E conversions, but the middle set of channels were hardwired for O-to-O connections (recall channels 4,5,6,7,8, and 9). However, not only were these channels wired directly between optical-in and optical-out through the driver ASIC and receiver ASIC bond pads, since the electrical signaling method was differential CML, the CML(+) pad of the driver ASIC was wirebonded to the CML(-) of the receiver ASIC for the same channel (and likewise the CML(-) was wirebonded to the CML(+)) thereby creating a logical inversion, as shown in figure 27. Therefore, if channel 4’s optical output was loop-backed to channel 4’s optical input using a single MT-to-MT parallel optical fiber ribbon cable, this channel would act as a free-running oscillator. The frequency would be governed by the total path length of the channel (and by thermal and noise effects as well), but the change of state would indicate the speed of the inner O-to-E / E-to-O conversion.

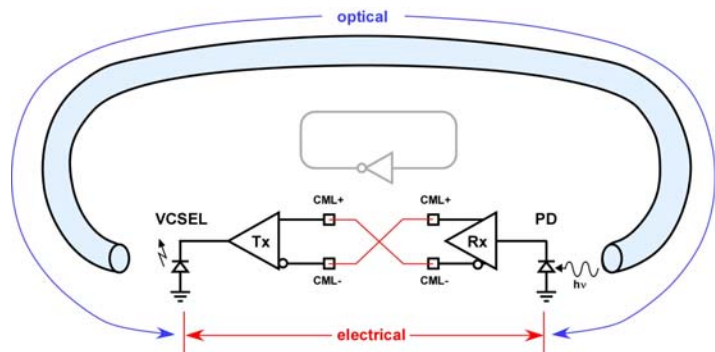


Figure 27: Schematic for Ring-Oscillator Test Setup

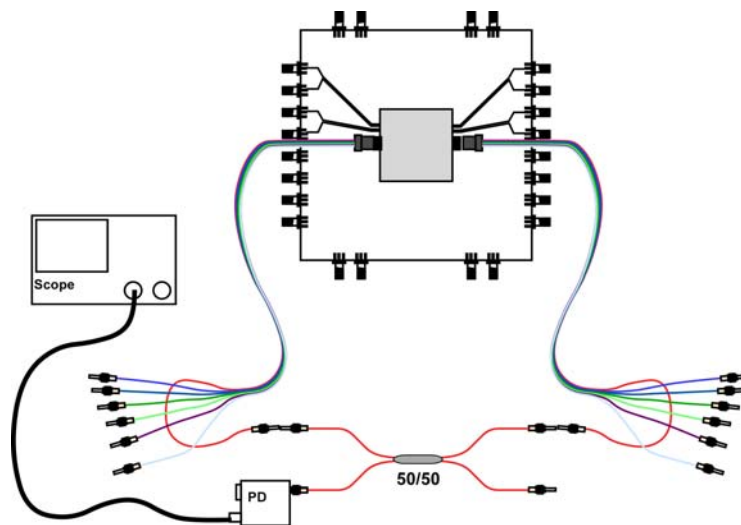


Figure 28: O-to-O Test Setup – Ring-Oscillator

The test setup shown in [figure 28](#) shows how the testboard and OEBGA IC Package were connected for the ring-oscillator configuration – note the absence of the Anritsu Data Generator. However, the most important feature of this setup, is the optical 50/50 splitter in the middle of the optical path. The oscillation is optically tapped and displayed on the Agilent scope (through the New Focus photodetector). Although the actual oscillation frequency is only about 25-MHz, optical tapping of the signal preserves the rising and falling edges of this signal – whereas electrical splitting could not without active devices and proper transmission line terminations.

In [figures 29 and 30](#), the square-wave oscillation pattern and the rising edge of the square-wave are shown, respectively. Note that the oscillation is somewhat noisy and actually changed oscillation frequency over time – this is the nature of the free-running oscillator and variations are mostly due to thermal noise. Note also that it was difficult to obtain a proper trigger signal from the free-running oscillator for the Agilent scope. Therefore, the electrical signal from the New Focus photodetector had to be electrically split using a Mini-Circuits 3-terminal power splitter – this halves the voltage swing, but matches the impedances of the transmission lines although incurring a small rise/fall time penalty. This also contributes to the noisy signal.

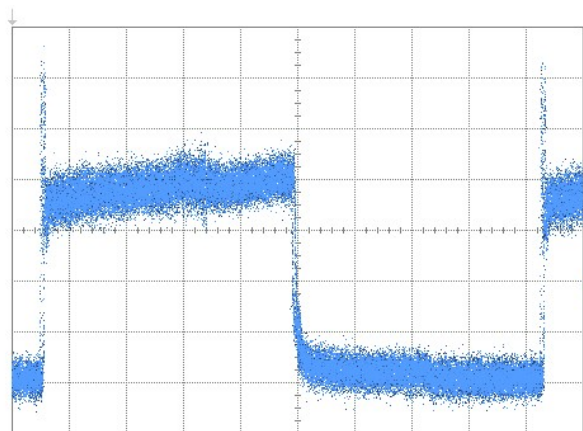


Figure 29: Oscillation Square-Wave for the OEBGA Ring Oscillator

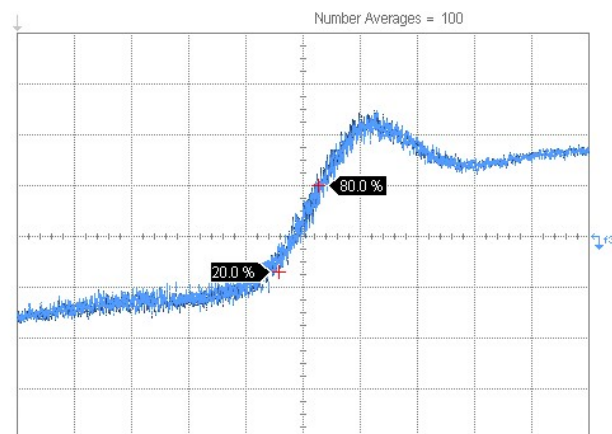


Figure 30: Rising-Edge for the OEBGA Ring Oscillator

The average oscillation frequency was 23-MHz (a period of 43.478 ns) and had a rising edge of 77.6 ps. Furthermore, the electrical delay (from PD to VCSEL inside the OEBGA) can also be calculated knowing the optical path length and the speed of light in an optical fiber; in this case the length was 8.647-m and the speed was 2.04×10^8 m/s (3×10^8 m/s / 1.47). Combining these two values with the period of the square wave, the delay through the OEBGA IC Package was calculated to be 0.975 ns. (Note that the mode of oscillation of the free-running oscillator was actually “n=2”, i.e.: there were two pulses traveling around the ring – this was the preferred operating mode of the oscillator).

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3. Summary:

Fundamentally, this first prototype Optically-Enabled BGA IC Package is the same as any other IC package except it has the value added feature of optical input and output ports on the sides of the package. This dramatically increases the overall bandwidth of the package since the total bandwidth also includes the electrical BGA solder-ball connections. Furthermore, the number of optical channels and optical ports (groupings of optical channels in a single connector) can be increased from the 2-port, 12-channels/port version described here up to an 8 port, 16 channels/port OEBGA IC Package where each channel is running at 10-Gbps – for a total of 1.28-Terabits/sec optically. This technology also leads to much longer signaling distances since optical fiber does not suffer from the same attenuation and dispersion as electrical signals. This also reduces possible EMI and EMR effects by containing the electrical signals safely within the IC package.

All of these features allow the interconnect to scale with the speed of the silicon processing without changing the fundamental assembly techniques involved in producing IC packages or Printed Circuit Board manufacturing and board population. This technique is truly “**fiber-to-the-chip**” (FTTC) without disrupting *the chip* – by bringing the optical signals within millimeters of the electrical signals of the chip.

The fundamental technology behind the optically enabled IC packages is the proprietary Reflex Photonics *LightABLE*[™] Optical Sub-Assembly (OSA). The OSA is a compact, multi-channel, planar module that provides electrical access on one-end and optical access on the other. It is pre-aligned so that the optical-to-electrical interface is registered to micron tolerances and then can be pick-and-placed into standard IC package platforms using standard assembly machines with 100-micron tolerances. The *LightABLE*[™] OSA is the work-horse for the OE-BGA concept and can be adapted to fit virtually any IC package strategy – cavity-up, cavity-down, BGA, PGA, organic or ceramic – that requires large amounts of data.

From the simple, low-cost evolution of the OSA and the subsequent OEBGA IC Package, Reflex Photonics has created a cost-effective, manufacturable method for producing Optically Enabled IC packages that are robust and can supply the interconnect bandwidth required by next generation processing chips.

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